NSWC Soft Switched Inverter Development Experience

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- This work was funded by the Office of Naval Research under the Power Electronic Building Block Program
- The goal of the PEBB program is to enable the application of more electric power conversion for US Navy ships through the affordable implementation of advanced electrical power conversion techniques and components.

- NSWC was tasked to investigate the use of soft switching inverter technology in a multifunctional electrical power converter.
- Concurrently, ONR tasked Harris Semiconductor to team with NSWC to produce the core building blocks comprising the converter.

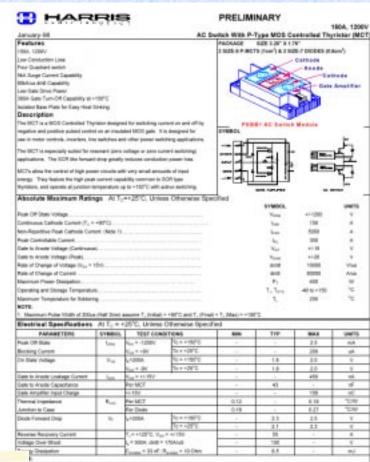
- Chosen topology Auxiliary Resonant Commutated Pole (ARCP) zero voltage switching inverter
 - Navy had previously worked with GECR&D on ARCP as a candidate for DC-AC ship service inverter module (SSIM) application under the Navy's Integrated Power System (IPS) Program.
- NSWC used the GE design as its starting point using core elements produced by Harris

- ARCPs that have been built at NSWC
 - PEBB1 based
 - pMCTs as both main and auxiliary switches
 - IGBT main switches, pMCT auxiliary switches
 - PEBB1.5 based
 - Non-punch-through IGBT main switches, combination of p and nMCT auxiliary switches

- PEBB1 Core Devices
 - Half Bridge Module
 - pMCTs
 - npt IGBTs
 - AC Module
 - pMCT
 - Gate Drive
 - Includes Jumper for Zero Voltage
 Turn-on Logic for Half Bridge
 - Water Cooled Heatsink



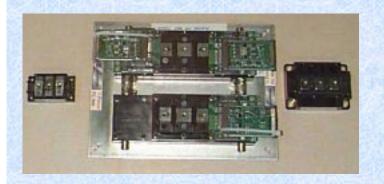


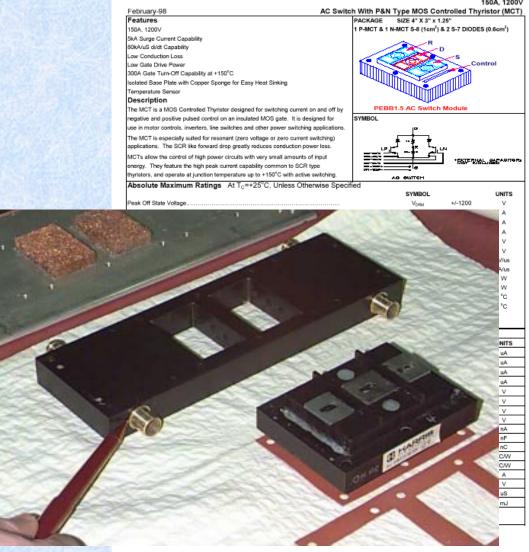


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auton. Prelimenry Sets. State shown is subject to charge

- PEBB1.5 Core Devices
 - Half Bridge Module
 - npt IGBTs
 - AC Module
 - one pMCT one nMCT
 - snubber resistor
 - Gate Drives
 - Heat Sink Assembly



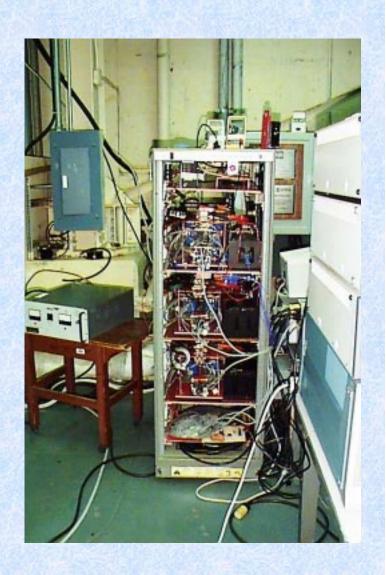


PRELIMINARY

HARRIS

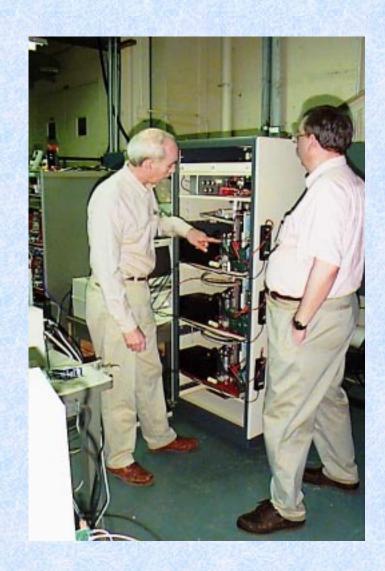
PEBB 1 Hardware

- Qty of 4 three phase units
 - Main switch PMCT
 - Aux Switch PMCT
 - DC Bus Caps orig. 7000uF
 - reduced to 3500uF per phase
 - Resonant inductor 1.6uH
 - Resonant Cap .8uf per switch
 - 1.6uf total per phase
 - Resonant frequency ~ 100kHz
 - Output filter 175uH, 50uF
 - Controller TMS320 DSP
 - 100ns step control of ac switch on time
 - at 800vdc = 40 amp step control



PEBB 1.5 ARCP Inverter

- Design Specifications: DC-AC operating mode
 - Input: 750 850Vdc
 - Output: 450Vac RMS at 250kW (water cooled)
- Major Components
 - Main switch NonPunchThrough IGBT
 - Aux. Switch Combo N-and P-MCT
 - DC Bus Caps 6900 uF per phase
 - Resonant inductor 1.0-1.2 uH
 - Resonant Cap .1 uF/switch, .2uF/phase
 - DSP Based Digital Controller
 - 100ns step control of ac switch on time
 - at 800vdc = 40 amp step control
- Present status
 - Assembly completed 4/3/98
 - Tested up to 200kW 10/98



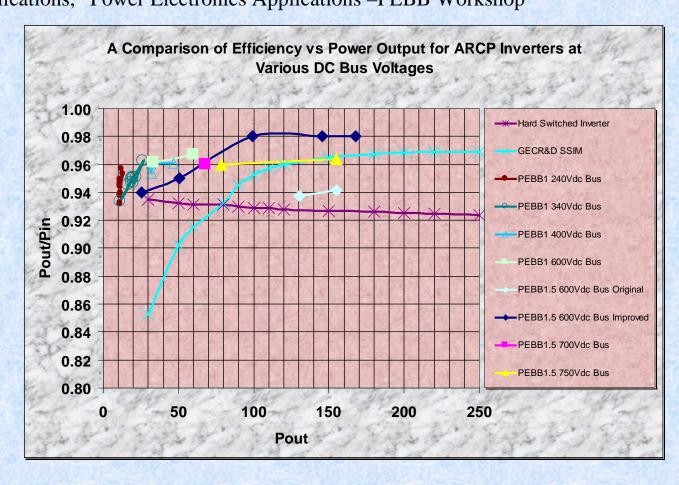
- Lower Loss/Higher Efficiency
- Lower Device Stress, Lower High Frequency EMI, Friendlier to the load in terms of dV/dt and dI/dt

- Lower Loss/Higher Efficiency
 - An ARCP inverter was designed built and tested by PSU under NSWC PEBB contract to investigate high frequency converter issues
 - IGBT Main switches/FET auxiliary
 - ARCP operation 190V, 14A output 63.4 kHz switching frequency
 - Disabled auxiliary circuit and operated as hard switched inverter at same output voltage and current
 - Switching frequency slowly increased until failure occurring at 32.5kHz
 - [1] Salberta, Frederick; Mayer, Jeffrey S.; and Cooley, Roger T., "An improved Control Strategy for a 50kHz Auxiliary Resonant Commutated Pole Converter," Power Electronics Specialist Conference St Louis MO June 22-27th 1997

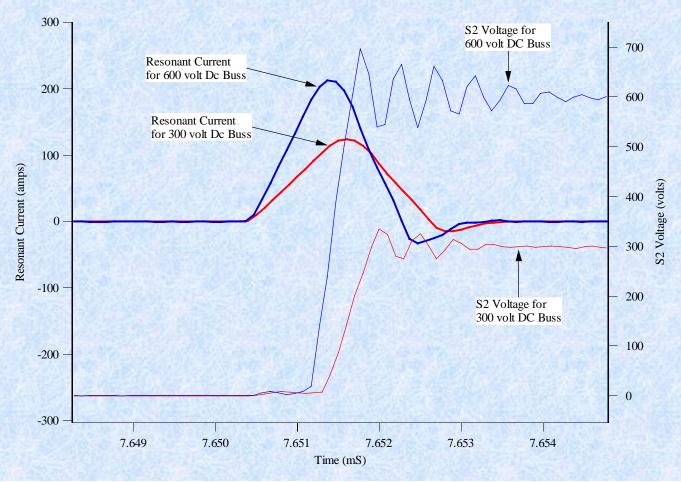
Lower Loss/Higher Efficiency

• [2] Keraluwala, Mustansir; Szczesny Paul; Esser, Albert and Hegner, Henry, "Development of a 250kVA, High Performance, Ship Service Inverter Module (SSIM) for Future Naval Applications," Power Electronics Applications –PEBB Workshop

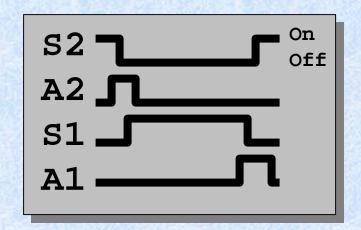
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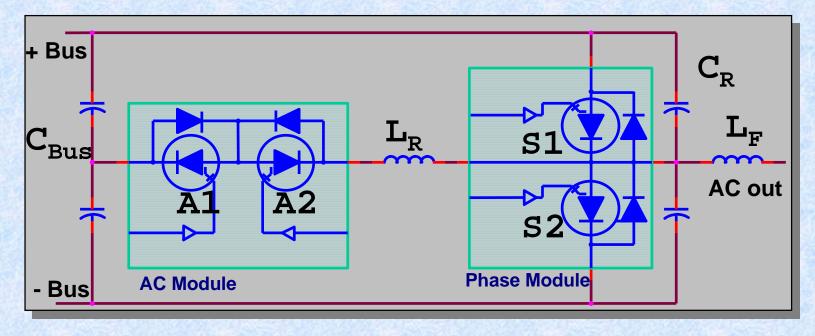


• Lower Device Stress, Lower High Frequency EMI, Friendlier to the load in terms of dV/dt and dI/dt

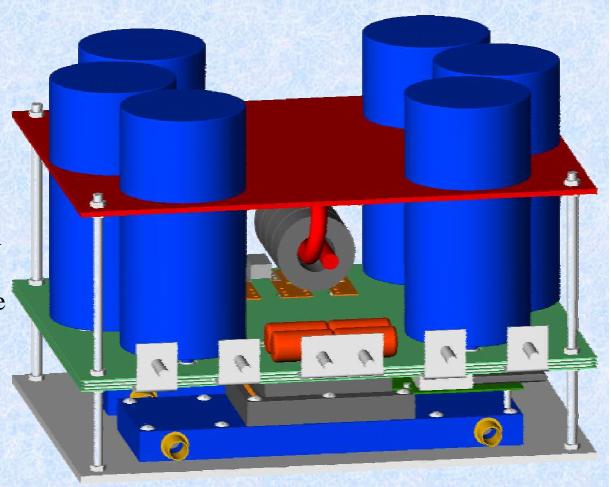


- Higher parts count
- Controller Complexity
- Higher cost





- Higher parts count
 - DC bus cap function
 - supply resonant current pulses (soft switching only)
 - supply HF ripple demanded by PWM (hard switch demand may be worse than soft switch due to the shape of the demanded voltage waveform -square wave vs trapezoid)
 - could end up being a wash



- Parts Count Resonant Inductor
 - − L value relatively low ~ 1.0 1.5uH
 - High frequency current components
 - Litz wire used
 - L value subject to variability in manufacture
 - L value subject to variability under operation due to temperature fluctuations (this has not yet been measured)
 - Not having a stable value inductor limits how close controller can push safety margins

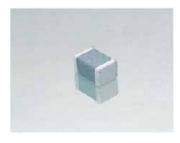


- Parts Count Resonant Capacitor
 - Requires accurate known value with little or no temperature drift
 - Quantity needed
 dependent on tail current
 of Phase switch
 - Expensive



NPO Dielectric General Specifications





NPO is the most popular formulation of the "temperature-compensating," EIA Class I ceramic materials. Modern NPO formulations contain neodymium, samarium and other rare earth oxides.

NPO ceramics offer one of the most stable capacitor dielectrics available. Capacitance charge with temperature is 0 ± 30 ppm°C which is less than $\pm 0.3\%$ Δ C from ± 55 °C to ± 125 °C. Capacitance drift or hysteresis for NPO ceramics is negligible at less than $\pm 0.05\%$ versus up to $\pm 2\%$ for films. Typical capacitance change with life is less than $\pm 0.1\%$ for NPOs, one-fifth that shown by most other dielectrics. NPO formulations show no aging characteristics.

The NPO formulation usually has a "Q" in excess of 1000 and shows little capacitance or "Q" changes with frequency. Their dielectric absorption is typically less than 0.6% which is similar to mice and most films.

Part Number (see page 3 for complete information and options)

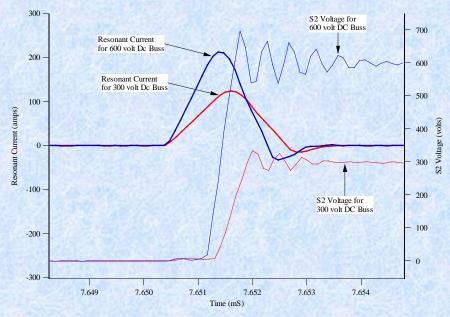


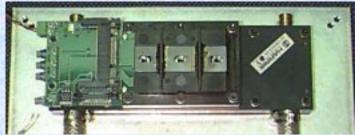
Performance Characteristics: NPO

Capacitance Range	0.5 pF to .033 μF (1.0 ±0.2 Vrms, 1kHz, for ≤100 pF use 1 MHz)
Capacitance Tolerances	Preferred ±5%, ±10% others available: ±25 pF, ±5 pF, ±1% (≥25pF), ±2%(≥13pF), ±20% For values ≤ 10 pF preferred tolerance is ±.5 pF, also available ±.25 pF.
Operating Temperature Range	-55°C to +125°C
Temperature Characteristic	0 ± 30 ppm/°C
Voltage Ratings	25, 50, 100 & 200 VDC (+125°C)
Dissipation Factor and "Q"	For values >30 pF: 0.1% max. (+25°C and +125°C) For values ≤30 pF: "Q" = 400 + 20XC (C in pF)
Insulation Resistance (+25°C, RVDC)	100,000 megohms min. or 1000 MΩ - μF min., whichever is less
Insulation Resistance (+125°C, RVDC)	10,000 megohms min. or 100 MΩ - μF min., whichever is less
Dielectric Strength	250% of rated voltage for 5 seconds at 50 mamp max, current
Test Voltage	1 ± 0.2 Vrms
Test Frequency	For values ≤100 pF: 1 MHz For values >100 pF: 1 KHz

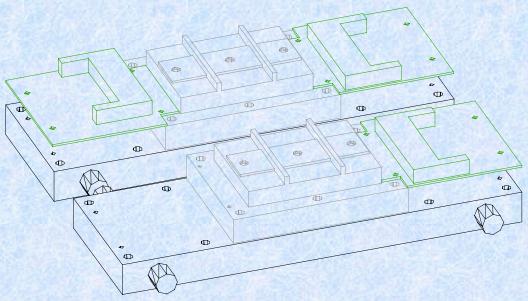
- Parts Count Auxiliary switch
 - needs to supply very high di/dt pulse
 - zero current turn off
 - PEBB1 and PEBB1.5 variants







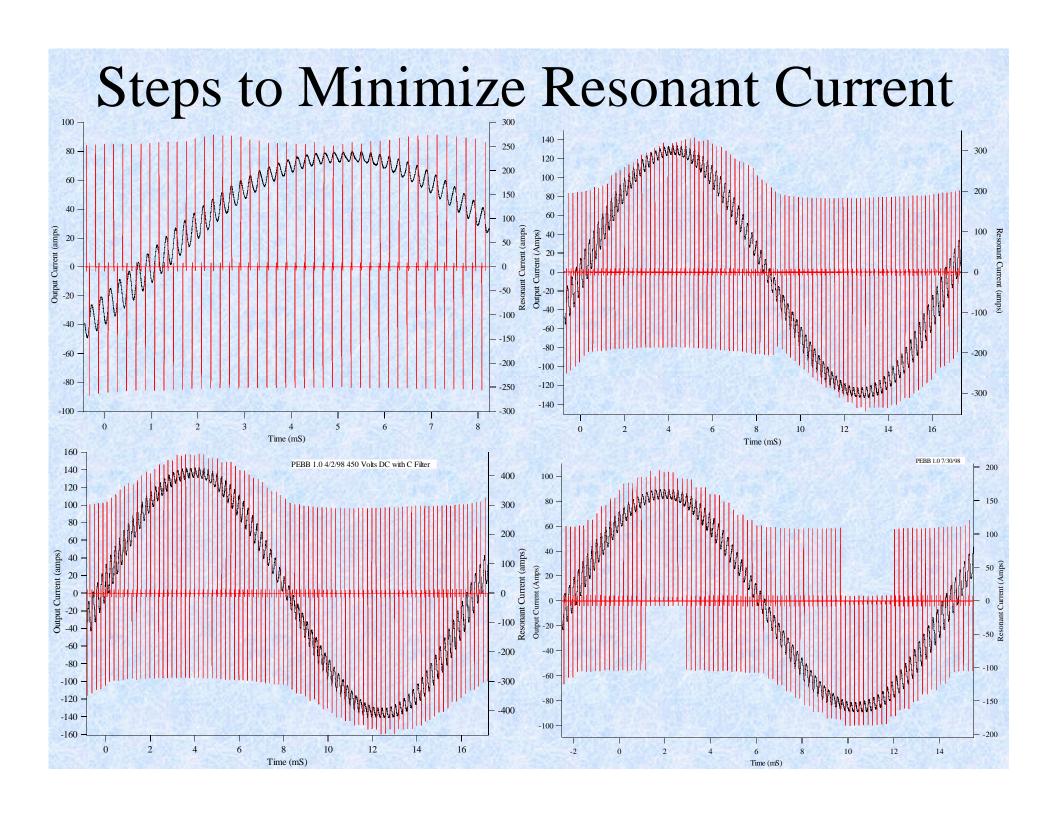
- Parts Count feedback signals needed
 - Soft Switch Transition
 - Vdc low bandwidth, 1% resolution
 - Ioutput 3 samples within 120 degrees of switching frequency, 12 bit resolution
 - Voltage Regulation
 - Vout update at switching frequency, 1% resolution



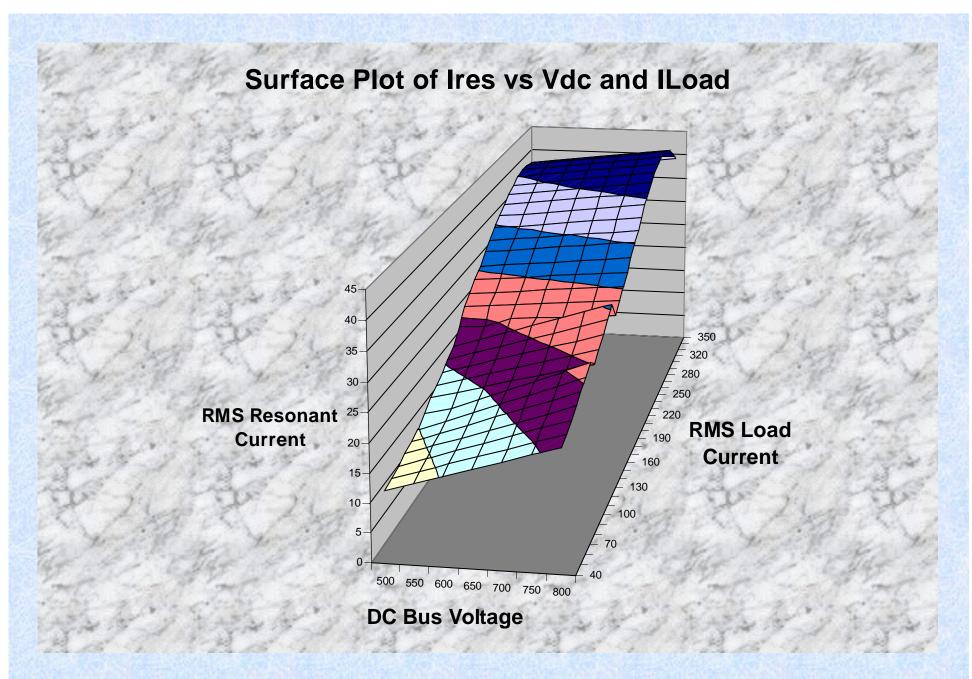
Higher cost

- The goal of the PEBB program is to develop an automated manufacturing process using pick and place assembly techniques to produce a module employing the proper types of semiconductor switches, diodes and ultimately passive and control components interconnected in the circuit topology requested by the circuit designer
- Harris PEBB1.5 modules employing HTP semiconductor die in a generic, user definable arrangement begin to demonstrate a way of removing the costly hand assembly process from power converter manufacturing

- A significant amount of effort was made in order to minimize the cost and size impact of the additional components required for ARCP
- The key was to supply the minimum amount of resonant energy to allow a zero voltage transition to occur
- This would minimize the current handling requirements of the additional components



Steps to Minimize Resonant Current 140 120 -150 -120 -140 --100 -400 350 Time (mS) 600 Time (mS) 600 350 300 500 500 300 250 400 200 150 -200 -250 -250 -300 -300 -Time (mS)



Projects to approximately 50A rms resonant current for full 250kW

Issues uncovered during analysis and testing

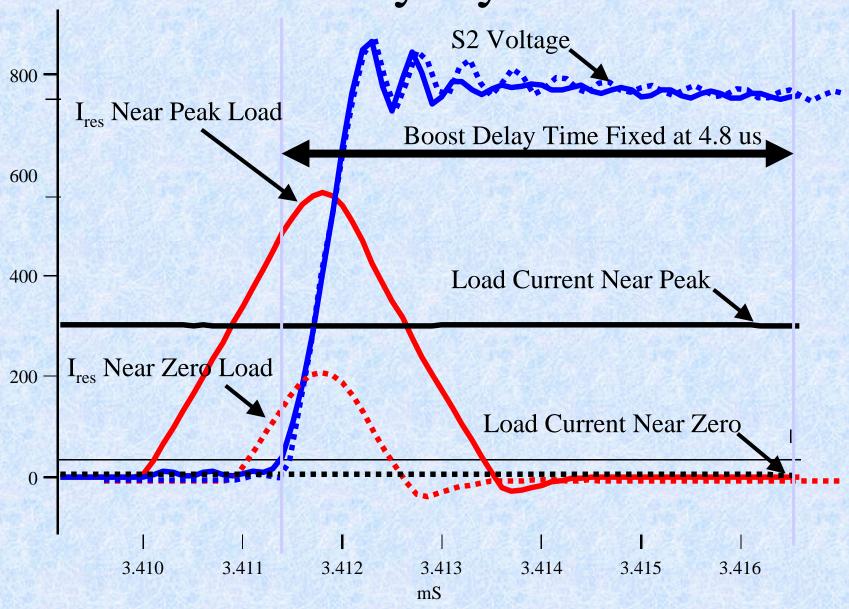
- Output filter design and manufacturing
 - hard to find inexpensive, compact, high frequency,
 high power inductors



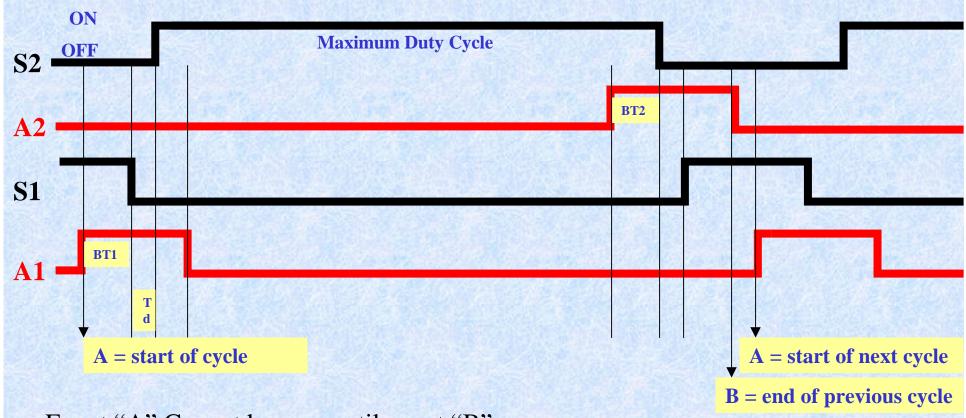
Issues uncovered during analysis and testing

- Present Controller Implementation has data sampling latency times which compromise performance
- Loss of duty cycle due to resonant pulse times and above latency times
- Difficult to design into controller enough safety margins to operate within real world limitations of chosen devices, yet have enough performance to compete with a hard switched converter

Maximum Duty Cycle Limitation



Maximum Duty Cycle Limitation



Event "A" Cannot happen until event "B" occurs

Event "B" cannot complete until resonant current pulse = 0

That time is not readily known, so a worst case Boost delay time of 4.8us is used

Maximum Duty Cycle Limitation

$$V_{LL} = 0.612 * V_{dc}[2d \text{ max} - 1]$$

- It is estimated that next generation controller will enable reducing latencies and dead times by up to 5us.
- A 10% improvement in duty cycle utilization corresponds to a 20% improvement in available Line to Line Voltage
- Note: Third Harmonic Injection will increase $V_{\rm LL}$ by 15%

Conclusion

- The NSWC PEBB as presently implemented as an ARCP inverter has been demonstrated at 200kW.
- On-going refinements are continuing, which allow the ARCP to achieve higher performance and multiple power conversion functions.

Conclusion

- The areas where improvements can be made to narrow the gap are:
 - A method of partitioning ARCP-specific control circuitry as close to the phaseleg as possible in order to allow traditional controllers to be employed
 - An automated module assembly process that would allow the ARCP to be easily manufactured with minimal hand assembly
 - less expensive high performance capacitors and inductors